

# 36V Radiation Hardened Dual Precision Operational Amplifier

## ISL70227SEH

The ISL70227SEH is a high precision dual operational amplifier featuring very low noise, low offset voltage, low input bias current and low temperature drift. These features plus its radiation tolerance, make the ISL70227SEH the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of precision, low noise and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision and analytical instrumentation, active filters, and power supply controls.

The ISL70227SEH is available in a 10 lead hermetic ceramic flatpack and operates over the extended temperature range of -55 °C to +125 °C.

## Applications

- Power supply control
- Industrial controls
- Active filter blocks
- Data acquisition

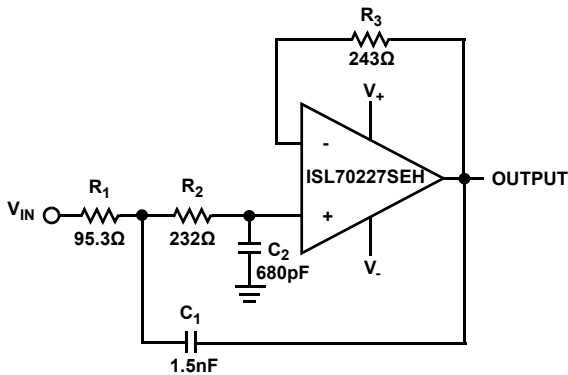
## Features

- Electrically screened to DLA SMD# [5962-12223](#)
- Wide supply range ..... 4.5V to 42V max.
- Very low voltage noise ..... 2.5nV/√Hz, typ.
- Gain-bandwidth product ..... 10MHz
- Superb offset drift ..... 1μV/°C, max
- Operating temperature range ..... -55 °C to +125 °C
- Low input voltage offset ..... 10μV, typ.
- Input bias current ..... 1nA, typ.
- Unity gain stable
- No phase reversal
- Radiation tolerance
  - High dose rate ..... 100krad(Si)
  - Low dose rate ..... 100krad(Si)\*
  - SEL/SEB LET<sub>TH</sub> (V<sub>S</sub> = ±18V) ..... 86.4MeV/mg/cm<sup>2</sup>
  - SEL immune (SOI process)

\* Product capability established by initial characterization. The EH version is acceptance tested on a wafer by wafer basis to 50krad(Si) at low dose rate.

## Related Literature

- [AN1669](#), "ISL70227SRH Evaluation Board User's Guide"
- [AN1756](#), "Single Events Effects Testing of the ISL70227SRH, Dual 36V Rad Hard Precision Operational Amplifiers"



SALLEN-KEY LOW PASS FILTER (1MHz)  
FIGURE 1. TYPICAL APPLICATION

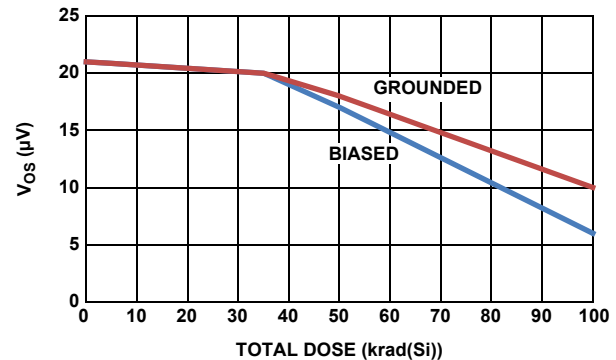


FIGURE 2. OFFSET VOLTAGE vs LOW DOSE RADIATION

# ISL70227SEH

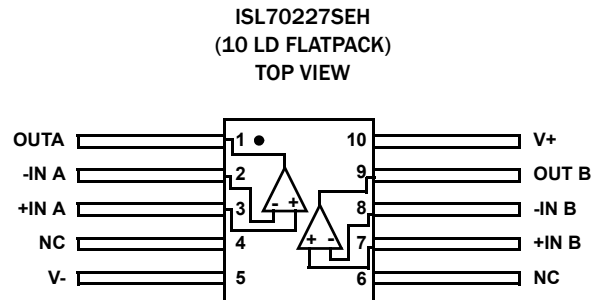
## Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962R1222301VXC (Note 1)	ISL70227SEHVF	-55 to +125	10 Ld Flatpack	K10.A
ISL70227SEHF/PROTO (Note 1)	ISL70227SEHF/PROTO	-55 to +125	10 Ld Flatpack	K10.A
5962R1222301V9A	ISL70227SEHVX	-55 to +125	Die	
ISL70227SEHX/SAMPLE	ISL70227SEHVX/SAMPLE	-55 to +125	Die	
ISL70227MHEVAL1Z	Evaluation Board			

### NOTES:

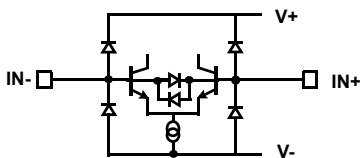
- These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

## Pin Configuration

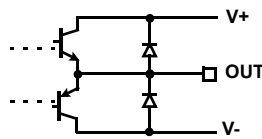


## Pin Descriptions

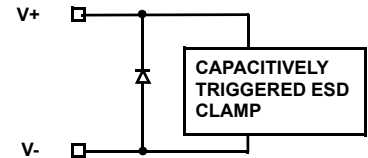
PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	+IN A	Circuit 1	Amplifier A Non-inverting Input
5	V-	Circuit 3	Negative Power Supply
7	+IN B	Circuit 1	Amplifier B Non-inverting Input
8	-IN B	Circuit 1	Amplifier B Inverting Input
9	OUT B	Circuit 2	Amplifier B Output
10	V+	Circuit 3	Positive Power Supply
1	OUT A	Circuit 2	Amplifier A Output
2	-IN A	Circuit 1	Amplifier A Inverting Input
4, 6	NC	-	Not Connected – This pin is not electrically connected internally.



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

# ISL70227SEH

## Absolute Maximum Ratings

Maximum Supply Voltage	42V
Maximum Supply Voltage (LET = 86.4 MeV • cm <sup>2</sup> /mg)	36V
Maximum Differential Input Current	20mA
Maximum Differential Input Voltage	0.5V
Min/Max Input Voltage	V <sub>-</sub> -0.5V to V <sub>+</sub> +0.5V
Max/Min Input Current for Input Voltage >V <sub>+</sub> or <V <sub>-</sub>	±20mA
Output Short-Circuit Duration (1 output at a Time)	Indefinite
ESD Tolerance	
Human Body Model (Tested per MIL-PRF-883 3015.7)	2kV
Machine Model (Tested per JESD22-A115-A)	300V
Charged Device Model (Tested per CDM-22C10ID)	750V
Di-electrically Isolated PR40 Process	Latch-up free

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
10 Ld Ceramic Flatpack (Notes 3, 4)	130	20
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see <a href="#">TB493</a>	

## Recommended Operating Conditions

Ambient Operating Temperature Range	-55°C to +125°C
Maximum Operating Junction Temperature	+150°C
Supply Voltage	4.5V (±2.25V) to 30V (±15V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For  $\theta_{JC}$ , the “case temp” location is the center of the ceramic on the package underside.

**Electrical Specifications**  $V_S \pm 15V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
$V_{OS}$	Offset Voltage		-75	-10	75	$\mu\text{V}$
			<b>-100</b>		<b>100</b>	$\mu\text{V}$
$TCV_{OS}$	Offset Voltage Drift		<b>-1</b>	0.1	<b>1</b>	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current		-10	1	10	nA
			<b>-12</b>		<b>12</b>	nA
$I_B$	Input Bias Current		-10	1	10	nA
			<b>-12</b>		<b>12</b>	nA
$V_{CM}$	Input Voltage Range	Guaranteed by CMRR	-13		13	V
			<b>-12</b>		<b>12</b>	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -13\text{V to }+13\text{V}$	115	120		dB
		$V_{CM} = -12\text{V to }+12\text{V}$	<b>115</b>			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25\text{V to } \pm 5\text{V}$	110	117		dB
		$V_S = \pm 3\text{V to } \pm 15\text{V}$	<b>110</b>			dB
$A_{VOL}$	Open-Loop Gain	$V_O = -13\text{V to }+13\text{V}$ $R_L = 10\text{k}\Omega$ to ground	1000	1500		V/mV
$V_{OH}$	Output Voltage High	$R_L = 10\text{k}\Omega$ to ground	13.5	13.65		V
			<b>13.2</b>			V
		$R_L = 2\text{k}\Omega$ to ground	13.4	13.5		V
			<b>13.1</b>			V
$V_{OL}$	Output Voltage Low	$R_L = 10\text{k}\Omega$ to ground		-13.65	-13.5	V
					<b>-13.2</b>	V
		$R_L = 2\text{k}\Omega$ to ground		-13.5	-13.4	V
					<b>-13.1</b>	V

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**Electrical Specifications**  $V_S \pm 15V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .** (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
$I_S$	Supply Current/Amplifier			2.2	2.8	mA
					<b>3.7</b>	mA
$I_{SC}$	Short-Circuit	$R_L = 0\Omega$ to ground		$\pm 45$		mA
$V_{SUPPLY}$	Supply Voltage Range	Guaranteed by PSRR	$\pm 2.25$		$\pm 15$	V
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product			10		MHz
$e_{n\text{-p-p}}$	Voltage Noise	0.1Hz to 10Hz		85		nV <sub>p-p</sub>
$e_n$	Voltage Noise Density	$f = 10\text{Hz}$		3		nV/ $\sqrt{\text{Hz}}$
$e_n$	Voltage Noise Density	$f = 100\text{Hz}$		2.8		nV/ $\sqrt{\text{Hz}}$
$e_n$	Voltage Noise Density	$f = 1\text{kHz}$		2.5		nV/ $\sqrt{\text{Hz}}$
$e_n$	Voltage Noise Density	$f = 10\text{kHz}$		2.5		nV/ $\sqrt{\text{Hz}}$
$i_n$	Current Noise Density	$f = 10\text{kHz}$		0.4		pA/ $\sqrt{\text{Hz}}$
THD + N	Total Harmonic Distortion + Noise	1kHz, $G = 1$ , $V_O = 3.5V_{RMS}$ , $R_L = 2\text{k}\Omega$		0.00022		%
<b>TRANSIENT RESPONSE</b>						
SR	Slew Rate	$A_V = 10$ , $R_L = 2\text{k}\Omega$ , $V_O = 4V_{P-P}$	$\pm 2.5$	$\pm 3.6$		V/ $\mu\text{s}$
			<b><math>\pm 2.0</math></b>			V/ $\mu\text{s}$
$t_r$ , $t_f$ , Small Signal	Rise Time 10% to 90% of $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 100\text{mV}_{P-P}$ , $R_f = R_g = 2\text{k}\Omega$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		36	100	ns
					<b>100</b>	ns
	Fall Time 90% to 10% of $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 100\text{mV}_{P-P}$ , $R_f = R_g = 2\text{k}\Omega$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		38	100	ns
					<b>100</b>	ns
$t_s$	Settling Time to 0.1% 10V Step; 10% to $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 10V_{P-P}$ , $R_g = R_f = 10\text{k}$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		3.4		$\mu\text{s}$
	Settling Time to 0.01% 10V Step; 10% to $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 10V_{P-P}$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		3.8		$\mu\text{s}$
$t_{OL}$	Output Overload Recovery Time	$A_V = 100$ , $V_{IN} = 0.2V$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		1.7		$\mu\text{s}$
OS+	Positive Overshoot	$A_V = 1$ , $V_{OUT} = 10V_{P-P}$ , $R_f = 0\Omega$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		20		%
					<b>35</b>	%
OS-	Negative Overshoot	$A_V = 1$ , $V_{OUT} = 10V_{P-P}$ , $R_f = 0\Omega$ , $R_L = 2\text{k}\Omega$ to $V_{CM}$		20		%
					35	%

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**Electrical Specifications**  $V_S \pm 15V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply across a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
$V_{OS}$	Offset Voltage		-75	-10	75	$\mu\text{V}$
			<b>-100</b>		<b>100</b>	$\mu\text{V}$
$TCV_{OS}$	Offset Voltage Drift		<b>-1</b>	0.1	<b>1</b>	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current		-10	1	10	nA
			<b>-25</b>		<b>25</b>	nA
$I_B$	Input Bias Current		-10	1	10	nA
			<b>-25</b>		<b>25</b>	nA
$V_{CM}$	Input Voltage Range	Guaranteed by CMRR	-13		13	V
			<b>-12</b>		<b>12</b>	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -13\text{V to }+13\text{V}$	<b>115</b>	120		dB
		$V_{CM} = -12\text{V to }+12\text{V}$	<b>115</b>			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25\text{V to } \pm 5\text{V}$	110	117		dB
		$V_S = \pm 3\text{V to } \pm 15\text{V}$	<b>110</b>			dB
$A_{VOL}$	Open-Loop Gain	$V_O = -13\text{V to }+13\text{V}$ $R_L = 10\text{k}\Omega$ to ground	1000	1500		V/mV
$V_{OH}$	Output Voltage High	$R_L = 10\text{k}\Omega$ to ground	13.5	13.65		V
			<b>13.2</b>			V
		$R_L = 2\text{k}\Omega$ to ground	13.4	13.5		V
			<b>13.1</b>			V
$V_{OL}$	Output Voltage Low	$R_L = 10\text{k}\Omega$ to ground		-13.65	-13.5	V
			<b>-13.2</b>			V
		$R_L = 2\text{k}\Omega$ to ground		-13.5	-13.4	V
			<b>-13.1</b>			V
$I_S$	Supply Current/Amplifier			2.2	2.8	mA
					<b>3.7</b>	mA
$I_{SC}$	Short-Circuit	$R_L = 0\Omega$ to ground		$\pm 45$		mA
$V_{SUPPLY}$	Supply Voltage Range	Guaranteed by PSRR	$\pm 2.25$		$\pm 15$	V
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product			10		MHz
$e_{np-p}$	Voltage Noise	0.1Hz to 10Hz		85		nV <sub>P-P</sub>
$e_n$	Voltage Noise Density	$f = 10\text{Hz}$		3		nV/ $\sqrt{\text{Hz}}$
$e_n$	Voltage Noise Density	$f = 100\text{Hz}$		2.8		nV/ $\sqrt{\text{Hz}}$
$e_n$	Voltage Noise Density	$f = 1\text{kHz}$		2.5		nV/ $\sqrt{\text{Hz}}$
$e_n$	Voltage Noise Density	$f = 10\text{kHz}$		2.5		nV/ $\sqrt{\text{Hz}}$
$i_n$	Current Noise Density	$f = 10\text{kHz}$		0.4		pA/ $\sqrt{\text{Hz}}$
THD + N	Total Harmonic Distortion + Noise	1kHz, $G = 1$ , $V_O = 3.5V_{RMS}$ , $R_L = 2\text{k}\Omega$		0.00022		%

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**Electrical Specifications**  $V_S \pm 15V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply across a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrads(Si)/s. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
<b>TRANSIENT RESPONSE</b>						
SR	Slew Rate	$A_V = 10$ , $R_L = 2k\Omega$ , $V_O = 4V_{P-P}$	$\pm 2.5$	$\pm 3.6$		V/ $\mu\text{s}$
			<b><math>\pm 2.0</math></b>			V/ $\mu\text{s}$
$t_r$ , $t_f$ , Small Signal	Rise Time 10% to 90% of $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 100mV_{P-P}$ $R_f = R_g = 2k\Omega$ , $R_L = 2k\Omega$ to $V_{CM}$		36	100	ns
					<b>100</b>	ns
	Fall Time 90% to 10% of $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 100mV_{P-P}$ $R_f = R_g = 2k\Omega$ , $R_L = 2k\Omega$ to $V_{CM}$			100	ns
					<b>100</b>	ns
$t_s$	Settling Time to 0.1% 10V Step; 10% to $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 10V_{P-P}$ $R_g = R_f = 10k$ , $R_L = 2k\Omega$ to $V_{CM}$		3.4		$\mu\text{s}$
	Settling Time to 0.01% 10V Step; 10% to $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 10V_{P-P}$ $R_L = 2k\Omega$ to $V_{CM}$		3.8		$\mu\text{s}$
$t_{OL}$	Output Overload Recovery Time	$A_V = 100$ , $V_{IN} = 0.2V$ , $R_L = 2k\Omega$ to $V_{CM}$		1.7		$\mu\text{s}$
OS+	Positive Overshoot	$A_V = 1$ , $V_{OUT} = 10V_{P-P}$ , $R_f = 0\Omega$ $R_L = 2k\Omega$ to $V_{CM}$		20		%
					<b>35</b>	%
OS-	Negative Overshoot	$A_V = 1$ , $V_{OUT} = 10V_{P-P}$ , $R_f = 0\Omega$ $R_L = 2k\Omega$ to $V_{CM}$		20		%
					<b>35</b>	%

**Electrical Specifications**  $V_S \pm 5V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
$V_{OS}$	Offset Voltage			-10		$\mu\text{V}$
$TCV_{OS}$	Offset Voltage Drift			0.1		$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current			1		nA
$I_B$	Input Bias Current			1		nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -3V$ to $+3V$		120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25V$ to $\pm 5V$		125		dB
$A_{VOL}$	Open-Loop Gain	$V_O = -3V$ to $+3V$ $R_L = 10k\Omega$ to ground		1500		V/mV
$V_{OH}$	Output Voltage High	$R_L = 10k\Omega$ to ground		3.65		V
		$R_L = 2k\Omega$ to ground		3.5		V
$V_{OL}$	Output Voltage Low	$R_L = 10k\Omega$ to ground		-3.65		V
		$R_L = 2k\Omega$ to ground		-3.5		V
$I_S$	Supply Current/Amplifier			2.2		mA
$I_{SC}$	Short-Circuit			$\pm 45$		mA

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**Electrical Specifications**  $V_S \pm 5V$ ,  $V_{CM} = 0$ ,  $V_O = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. **Boldface limits apply across the operating temperature range,  $-55^\circ C$  to  $+125^\circ C$ .** (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product			10		MHz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, $V_O = 2.5V_{RMS}$ , $R_L = 2k\Omega$		0.0034		%
<b>TRANSIENT RESPONSE</b>						
SR	Slew Rate	$A_V = 10$ , $R_L = 2k\Omega$		$\pm 3.6$		V/ $\mu s$
$t_r$ , $t_f$ , Small Signal	Rise Time 10% to 90% of $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 100mV_{P-P}$ $R_f = R_g = 2k\Omega$ , $R_L = 2k\Omega$ to $V_{CM}$		36		ns
	Fall Time 90% to 10% of $V_{OUT}$	$A_V = -1$ , $V_{OUT} = 100mV_{P-P}$ $R_f = R_g = 2k\Omega$ , $R_L = 2k\Omega$ to $V_{CM}$		38		ns
$t_s$	Settling Time to 0.1%	$A_V = -1$ , $V_{OUT} = 4V_{P-P}$ $R_f = R_g = 2k\Omega$ , $R_L = 2k\Omega$ to $V_{CM}$		1.6		$\mu s$
	Settling Time to 0.01%	$A_V = -1$ , $V_{OUT} = 4V_{P-P}$ $R_f = R_g = 2k\Omega$ , $R_L = 2k\Omega$ to $V_{CM}$		4.2		$\mu s$

NOTE:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

**High Dose Rate Post Radiation Characteristics**  $V_S \pm 15V$ ,  $V_{CM} = 0V$ ,  $V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

PARAMETER	DESCRIPTION	CONDITIONS	50k RAD	75k RAD	100k RAD	UNIT
$V_{OS}$	Offset Voltage		34	30	30	$\mu V$
$I_{OS}$	Input Offset Current		-1	-1	-2	nA
$I_B$	Input Bias Current		-1	-2	-3	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -13V$ to $+13V$	155	155	155	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.25V$ to $\pm 15V$	116	116	116	dB
$A_{VOL}$	Open-Loop Gain	$V_O = -13V$ to $+13V$ $R_L = 10k\Omega$ to ground	3500	3500	3500	V/mV
$I_S$	Supply Current/Amplifier		2.2	2.2	2.2	mA

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**Low Dose Rate Post Radiation Characteristics**  $V_S \pm 15V$ ,  $V_{CM} = 0V$ ,  $V_O = 0V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ C$ , unless otherwise noted. This data is typical test data post radiation exposure at a rate of  $10\text{mrad(Si)}/s$ . This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

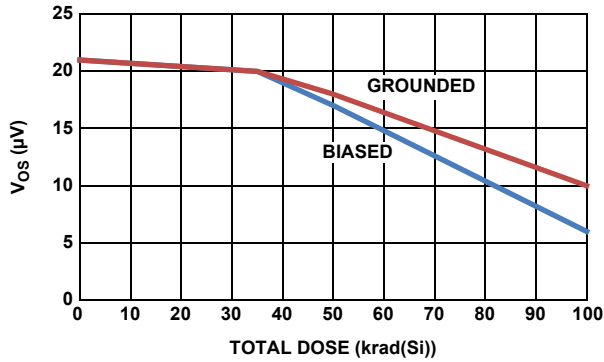


FIGURE 3. OFFSET VOLTAGE vs RADIATION

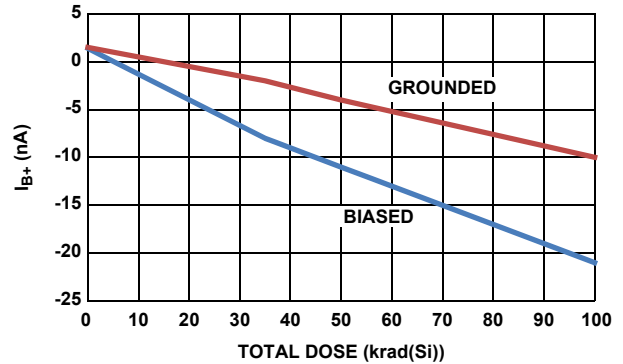


FIGURE 4. POSITIVE INPUT BIAS CURRENT vs RADIATION

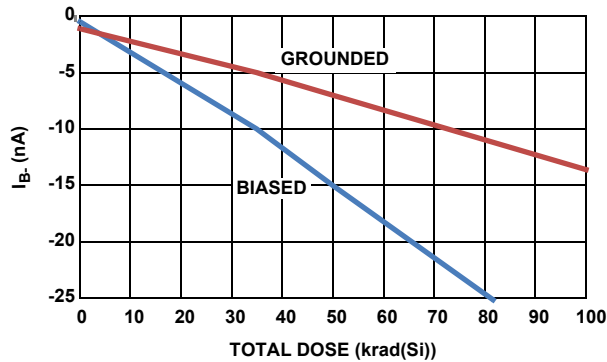


FIGURE 5. NEGATIVE INPUT BIAS CURRENT vs RADIATION

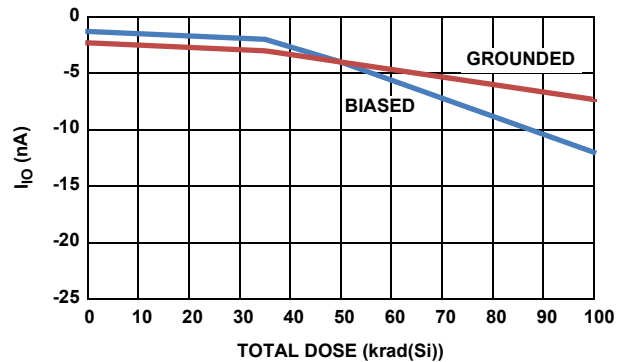


FIGURE 6. OFFSET CURRENT vs RADIATION

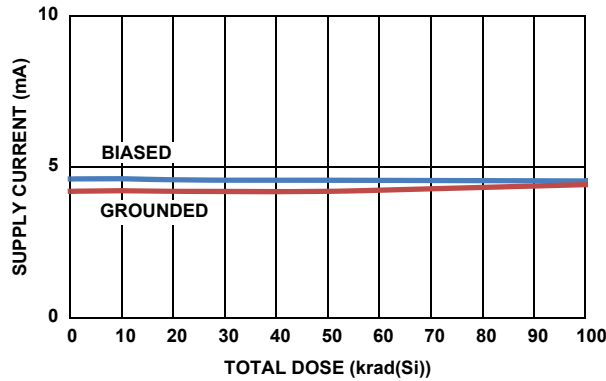


FIGURE 7. TOTAL SUPPLY CURRENT vs RADIATION



## Typical Performance Curves $V_S = \pm 15V, V_{CM} = 0V, R_L = \text{Open}, T_A = +25^\circ C$ , unless otherwise specified.

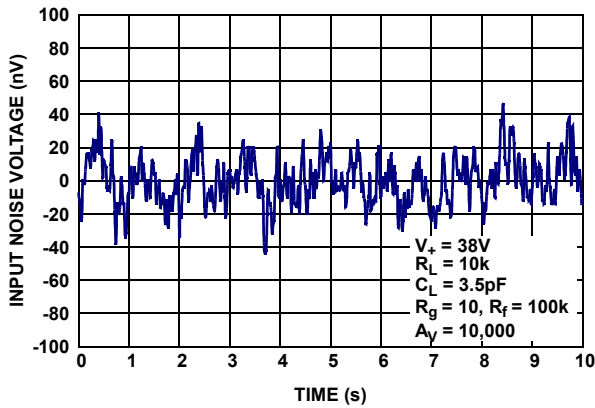


FIGURE 8. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

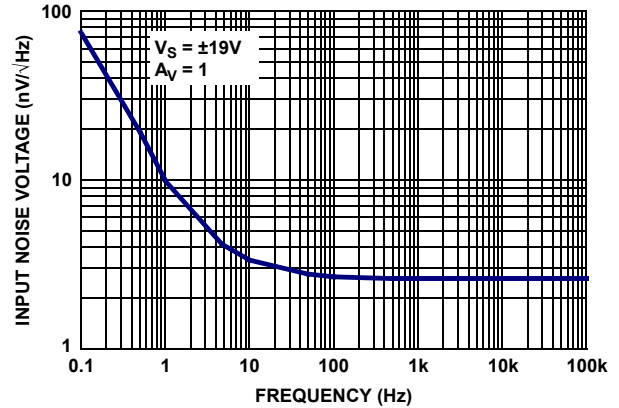


FIGURE 9. INPUT NOISE VOLTAGE SPECTRAL DENSITY

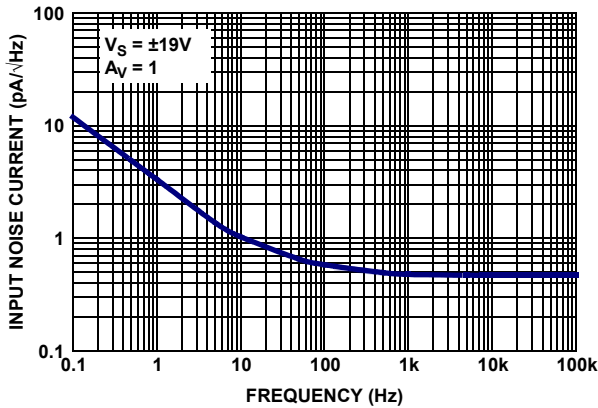


FIGURE 10. INPUT NOISE CURRENT SPECTRAL DENSITY

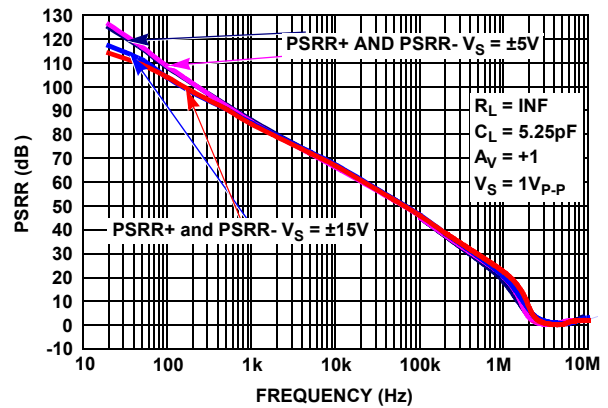


FIGURE 11. PSRR vs FREQUENCY,  $V_S = \pm 5V, \pm 15V$

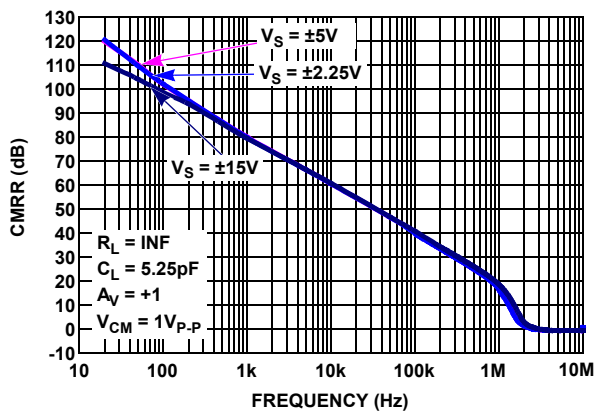


FIGURE 12. CMRR vs FREQUENCY,  $V_S = \pm 2.25V, \pm 5V, \pm 15V$

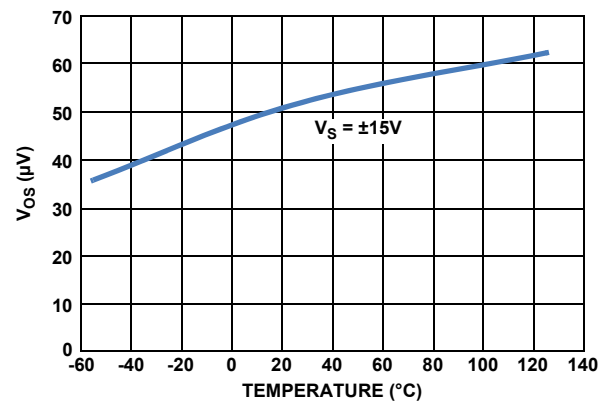


FIGURE 13.  $V_{OS}$  vs TEMPERATURE

## Typical Performance Curves $V_S = \pm 15V$ , $V_{CM} = 0V$ , $R_L = \text{Open}$ , $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

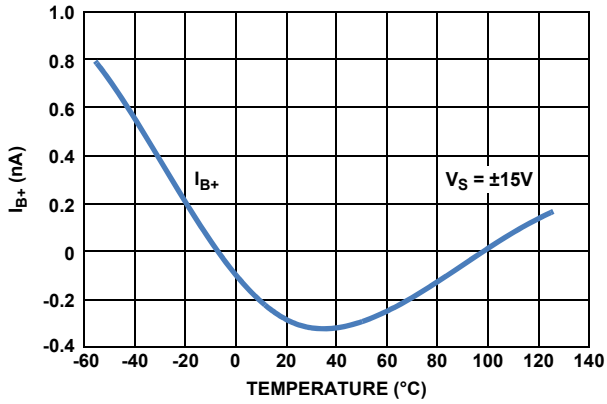


FIGURE 14.  $I_{B+}$  vs TEMPERATURE

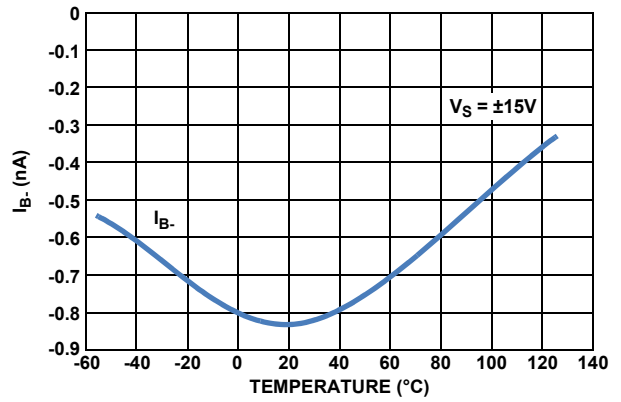


FIGURE 15.  $I_{B-}$  vs TEMPERATURE

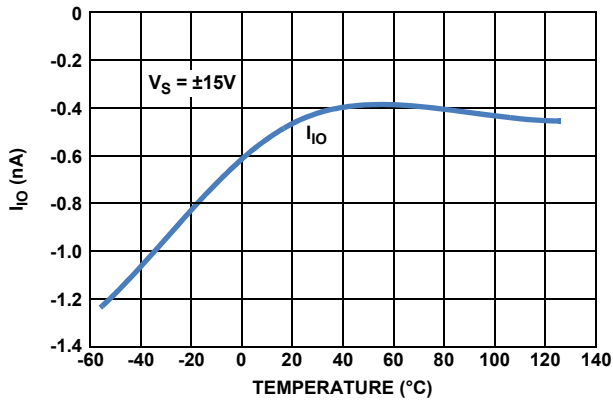


FIGURE 16.  $I_{IO}$  vs TEMPERATURE

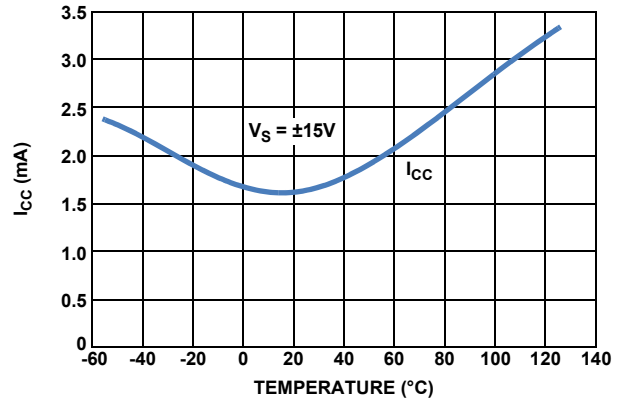


FIGURE 17. SUPPLY CURRENT vs TEMPERATURE

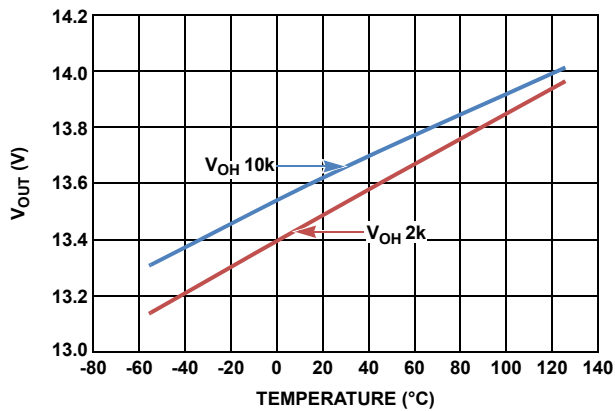


FIGURE 18.  $V_{OH}$  vs TEMPERATURE,  $V_S = \pm 15V$

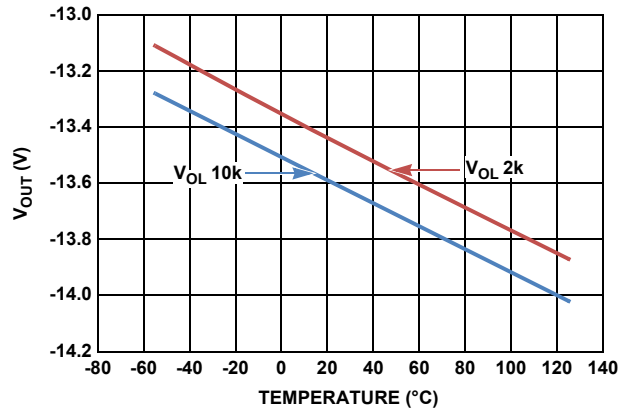


FIGURE 19.  $V_{OL}$  vs TEMPERATURE,  $V_S = \pm 15V$

## Typical Performance Curves $V_S = \pm 15V, V_{CM} = 0V, R_L = \text{Open}, T_A = +25^\circ C$ , unless otherwise specified. (Continued)

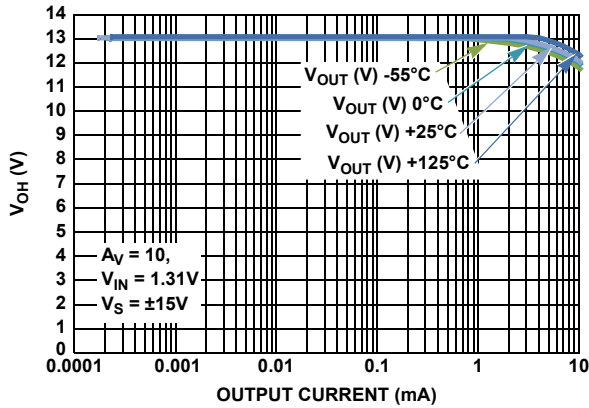


FIGURE 20.  $V_{OH}$  vs OUTPUT CURRENT

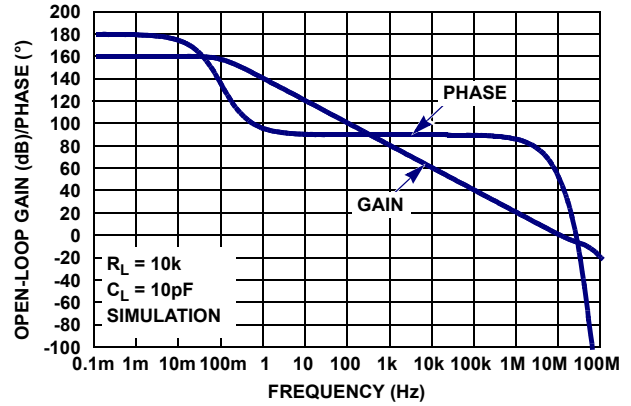


FIGURE 21. OPEN-LOOP GAIN, PHASE vs FREQUENCY,  $R_L = 10k\Omega, C_L = 10pF$

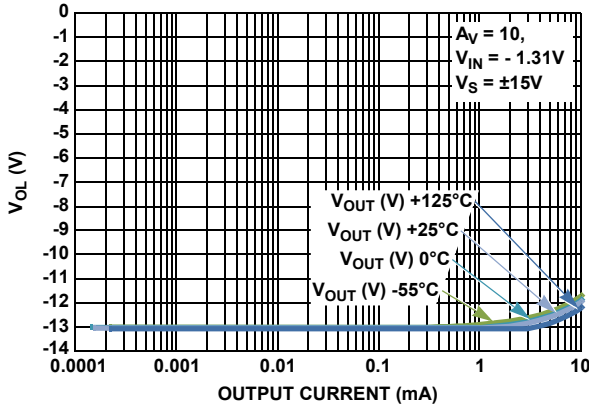


FIGURE 22.  $V_{OL}$  vs OUTPUT CURRENT

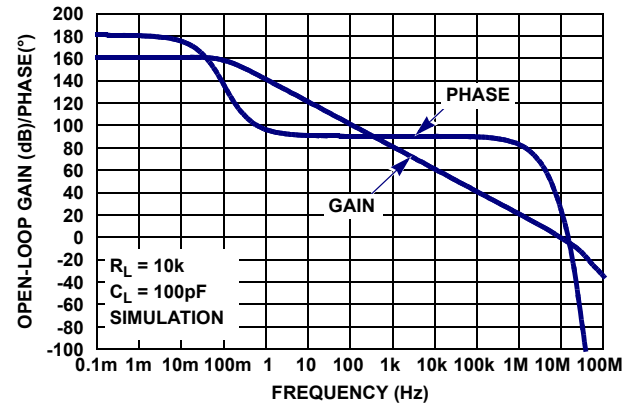


FIGURE 23. OPEN-LOOP GAIN, PHASE vs FREQUENCY,  $R_L = 10k\Omega, C_L = 100pF$

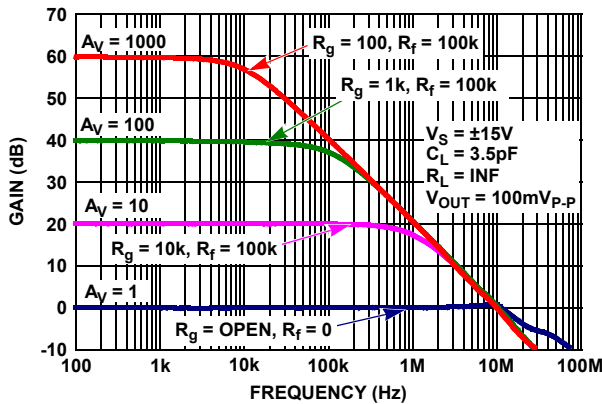


FIGURE 24. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

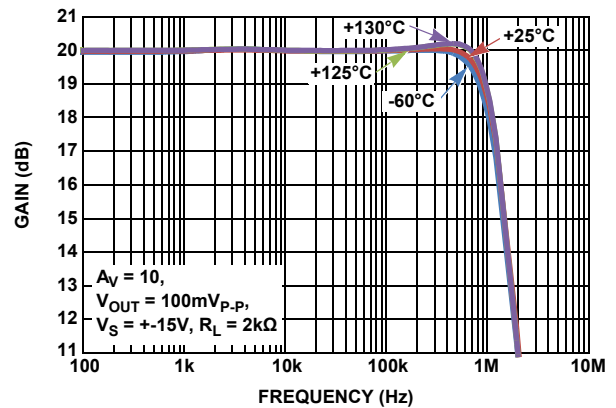


FIGURE 25. GAIN vs FREQUENCY vs TEMPERATURE

## Typical Performance Curves $V_S = \pm 15V, V_{CM} = 0V, R_L = \text{Open}, T_A = +25^\circ C$ , unless otherwise specified. (Continued)

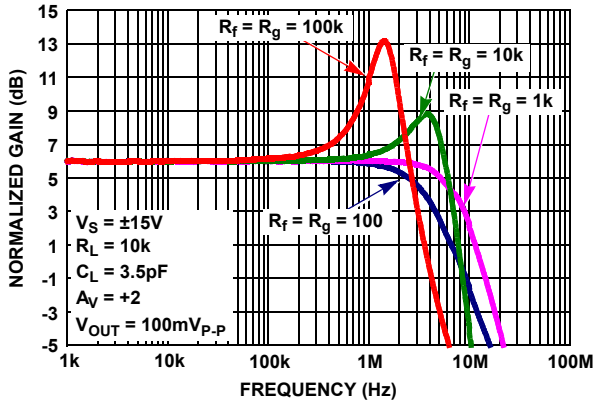


FIGURE 26. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE  $R_f/R_g$

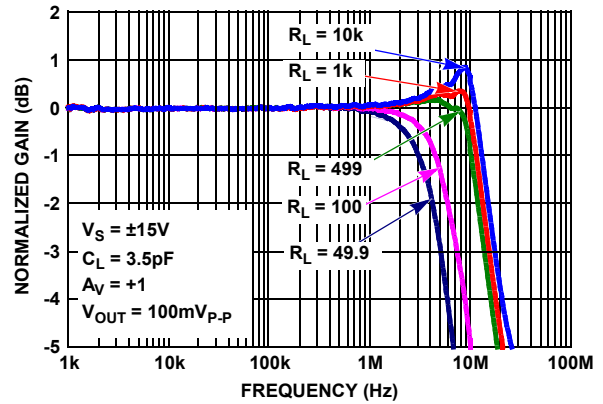


FIGURE 27. GAIN vs FREQUENCY vs  $R_L$

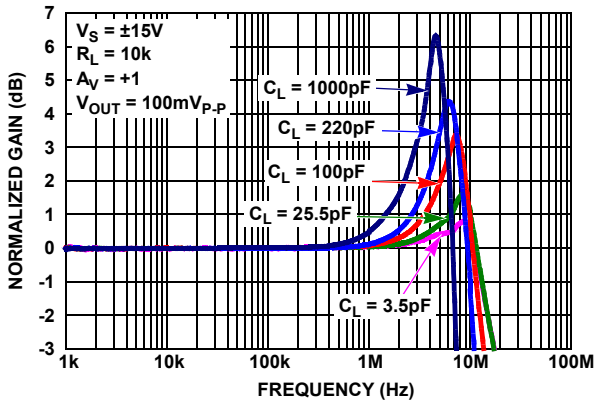


FIGURE 28. GAIN vs FREQUENCY vs  $C_L$

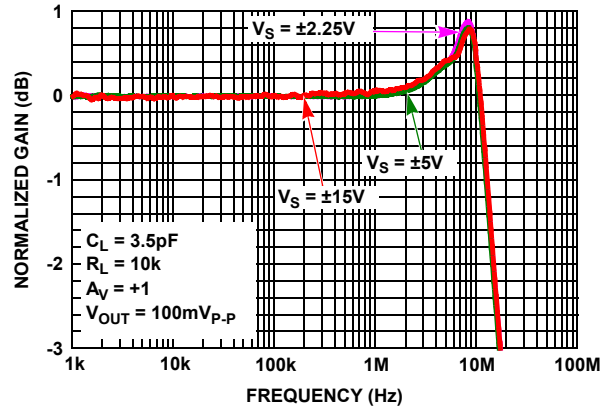


FIGURE 29. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

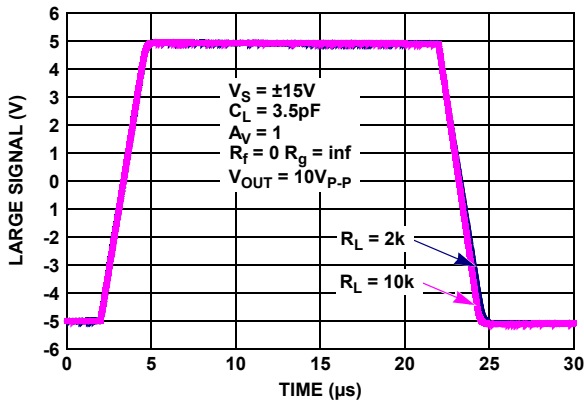


FIGURE 30. LARGE SIGNAL 10V STEP RESPONSE,  $V_S = \pm 15V$

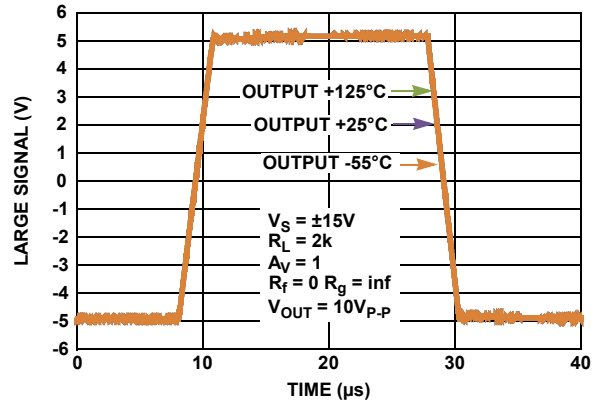


FIGURE 31. LARGE SIGNAL 10V STEP RESPONSE,  $V_S = \pm 15V$  vs TEMPERATURE

## Typical Performance Curves $V_S = \pm 15V, V_{CM} = 0V, R_L = \text{Open}, T_A = +25^\circ C$ , unless otherwise specified. (Continued)

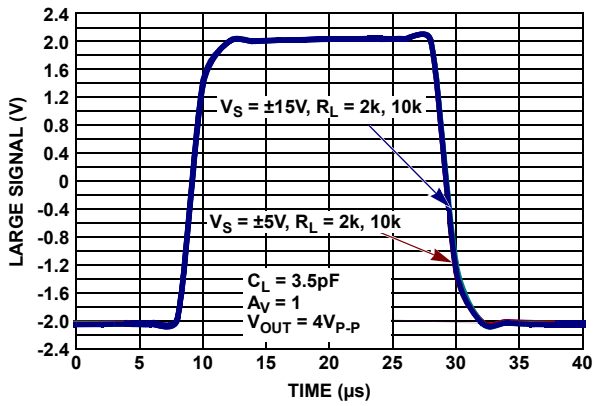


FIGURE 32. LARGE SIGNAL TRANSIENT RESPONSE vs  $R_L$ ,  $V_S = \pm 5V, \pm 15V$

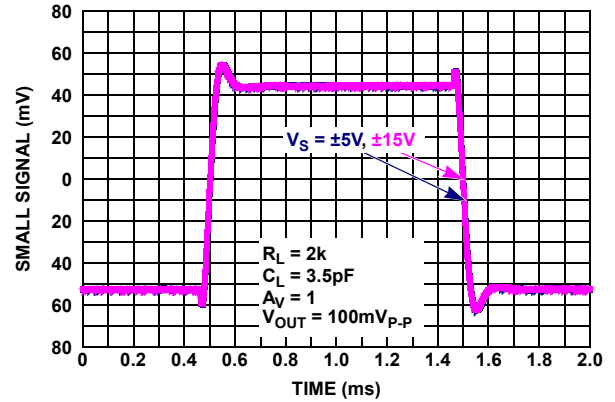


FIGURE 33. SMALL SIGNAL TRANSIENT RESPONSE,  $V_S = \pm 5V, \pm 15V$

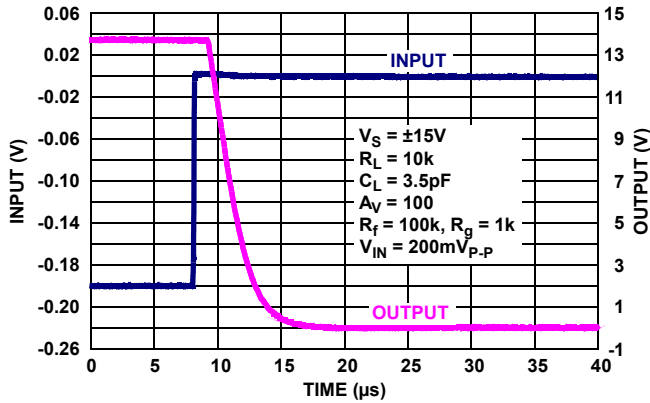


FIGURE 34. POSITIVE OUTPUT OVERLOAD RESPONSE TIME,  $V_S = \pm 15V$

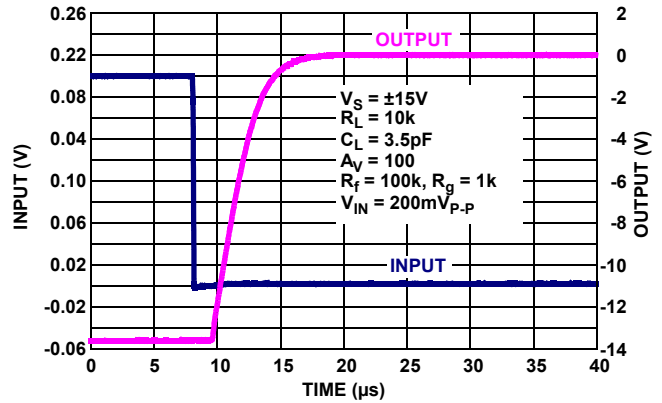


FIGURE 35. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME,  $V_S = \pm 15V$

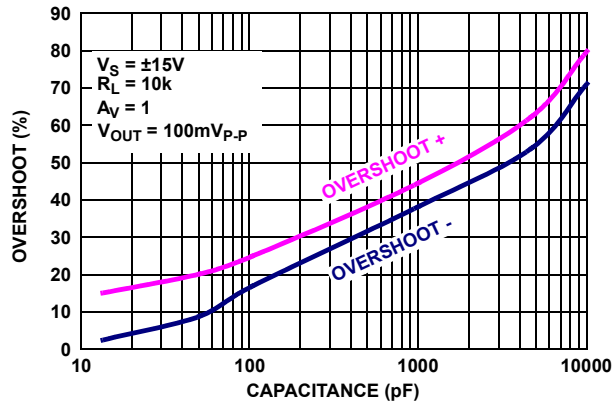


FIGURE 36. % OVERSHOOT vs LOAD CAPACITANCE,  $V_S = \pm 15V$

## Applications Information

### Functional Description

The ISL70227SEH is a dual, low noise 10MHz BW precision op amp fabricated in a new precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (1nA typical), low input offset voltage (10μV typ), low input noise voltage (3nV/√Hz), and low 1/f noise corner frequency (5Hz). These amplifiers also feature high open-loop gain (1500V/mV) for excellent CMRR (120dB) and THD+N performance (0.0002% at 3.5V<sub>RMS</sub>, 1kHz into 2kΩ). A complimentary bipolar output stage enables high capacitive load drive without external compensation.

### Operating Voltage Range

The devices are designed to operate over the 4.5V (±2.25V) to 36V (±18V) range and are fully characterized at 30V (±15V). Parameter variation with operating voltage is shown in the [“Typical Performance Curves”](#) beginning on [page 9](#).

### Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, and an additional anti-parallel diode pair across the inputs (see [Figures 37](#) and [38](#)).

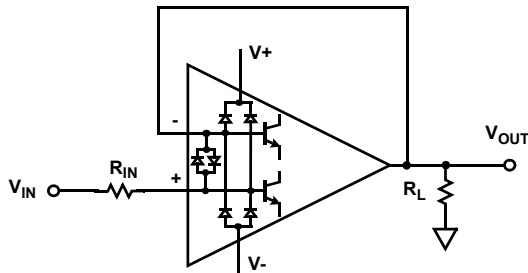


FIGURE 37. INPUT ESD DIODE CURRENT LIMITING - UNITY GAIN

For unity gain applications (see [Figure 37](#)) where the output is connected directly to the non-inverting input, a current limiting resistor ( $R_{IN}$ ) will be needed under the following conditions to protect the anti-parallel differential input protection diodes.

- The amplifier input is supplied from a low impedance source.
- The input voltage rate-of-rise ( $dV/dt$ ) exceeds the maximum slew rate of the amplifier ( $\pm 3.6V/\mu s$ ).

If the output lags far enough behind the input, the anti-parallel input diodes can conduct. For example, if an input pulse ramps from 0V to +10V in 1μs, then the output of the ISL70227SEH will reach only +3.6V (slew rate = 3.6V/μs) while the input is at 10V. The input differential voltage of 6.4V will force input ESD diodes to conduct, dumping the input current directly into the output stage and the load. The resulting current flow can cause permanent damage to the ESD diodes. The ESD diodes are rated to 20mA, and in the previous example; setting  $R_{IN}$  to 1kΩ resistor (see [Figure 37](#)) would limit the current to <6.4mA and provide additional protection of up to ±20V at the input.

In applications where one or both amplifier input terminals are at risk of exposure to high voltage, current limiting resistors may be needed at each input terminal (see [Figure 38](#)  $R_{IN+}$ ,  $R_{IN-}$ ) to limit current through the power supply ESD diodes to 20mA.

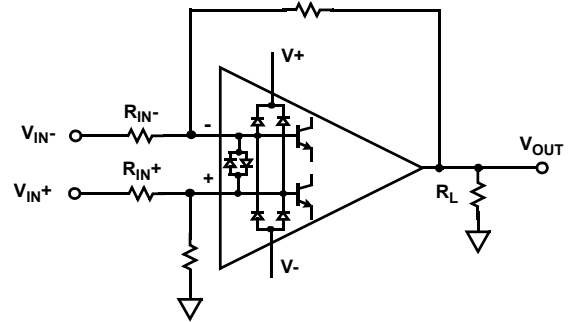


FIGURE 38. INPUT ESD DIODE CURRENT LIMITING - DIFFERENTIAL INPUT

### Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only one amplifier at a time. Continuous operation under these conditions may degrade long term reliability.

### Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70227SEH are immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

### Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature ( $T_{JMAX}$ ) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using [Equation 1](#):

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$  is the sum of the maximum power dissipation of each amplifier in the package ( $PD_{MAX}$ )
- $PD_{MAX}$  for each amplifier can be calculated using [Equation 2](#):

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- $T_{MAX}$  = Maximum ambient temperature
- $\theta_{JA}$  = Thermal resistance of the package
- $PD_{MAX}$  = Maximum power dissipation of one amplifier
- $V_S$  = Total supply voltage
- $I_{qMAX}$  = Maximum quiescent supply current of one amplifier
- $V_{OUTMAX}$  = Maximum output voltage swing of the application
- $R_L$  = Load resistance

# ISL70227SEH

## Package Characteristics

### Weight of Packaged Device

0.4029 grams (Typical)

### Lid Characteristics

Finish: Gold

Case Isolation to Any Lead:  $20 \times 10^9 \Omega$  (min)

## Die Characteristics

### Die Dimensions

$1565\mu\text{m} \times 2125\mu\text{m}$  (62mils x 84mils)

Thickness:  $355\mu\text{m} \pm 25\mu\text{m}$  (14 mils  $\pm$  1 mil)

### Interface Materials

#### GLASSIVATION

Type: Nitrox

Thickness:  $15\text{k}\text{\AA}$

### TOP METALLIZATION

Type: AlCu (99.5%/0.5%)

Thickness:  $30\text{k}\text{\AA}$

### BACKSIDE FINISH

Silicon

### PROCESS

Dielectrically Isolated Complementary Bipolar - PR40

## ASSEMBLY RELATED INFORMATION

### SUBSTRATE POTENTIAL

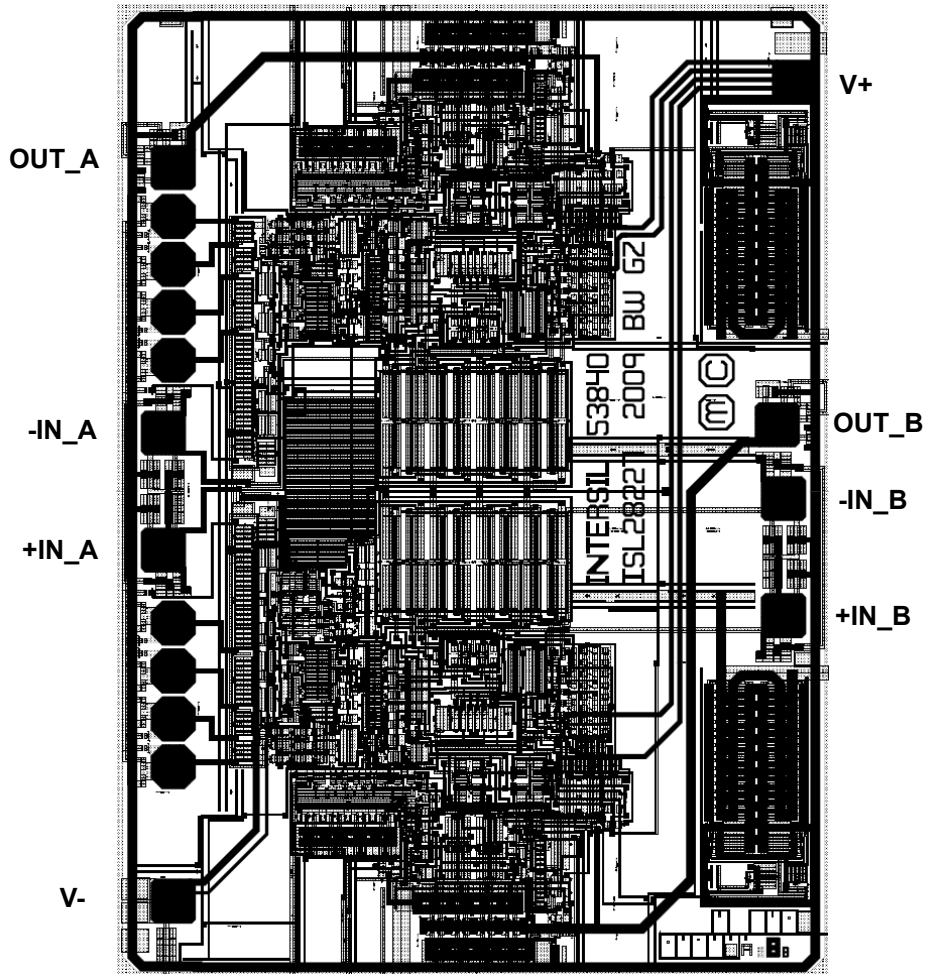
Floating

## ADDITIONAL INFORMATION

### WORST CASE CURRENT DENSITY

$< 2 \times 10^5 \text{ A/cm}^2$

## Metallization Mask Layout



# ISL70227SEH

TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )	dX ( $\mu\text{m}$ )	dY ( $\mu\text{m}$ )	BOND WIRES PER PAD
OUT_A	11	0	1530	70	70	1
-IN_A	13	-20.5	976	70	70	1
+IN_A	14	-20.5	732	70	70	1
V-	9	0	0	70	70	1
+IN_B	16	1272.5	595.5	70	70	1
-IN_B	15	1272.5	839.5	70	70	1
OUT_B	12	1259.5	993.5	70	70	1
V+	10	1295.5	1708	70	70	1

NOTE:

6. Origin of coordinates is the centroid of pad 9.



## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
July 18, 2014	FN7958.3	Updated "Radiation tolerance" on page 1 from: "SEL/SEB LETTH 86MeV • cm2/mg High dose rate 100krad(Si) Low dose rate 100krad(Si)*" to: "High Dose Rate100krad(Si) Low Dose Rate100krad(Si)* SEL/SEB LET <sub>TH</sub> (VS = ±18V)86.4MeV/mg/cm <sup>2</sup> SEL Immune (SOI Process)" Updated Odering Information on page 2 as follows: - Headings - Notes (Removed MSL note as it is not applicable to Hermetic packages and added SMD note) Replaced Figures 18 and 19. Updated About Intersil verbiage.
February 22, 2013	FN7958.2	Corrected ordering number on page 2 for ISL70227SEHVF from 5962R1222301VXA to 5962R1222301VXC.
August 24, 2012	FN7958.1	Initial release.

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

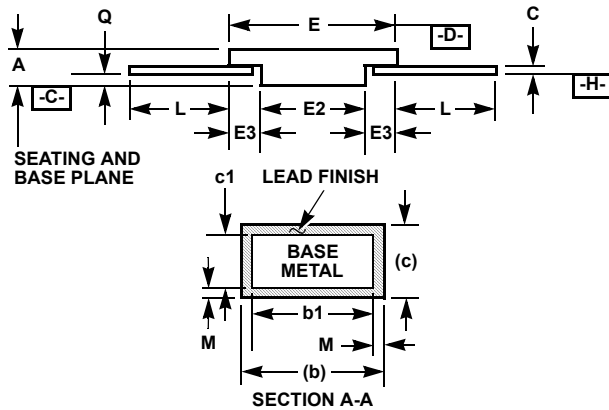
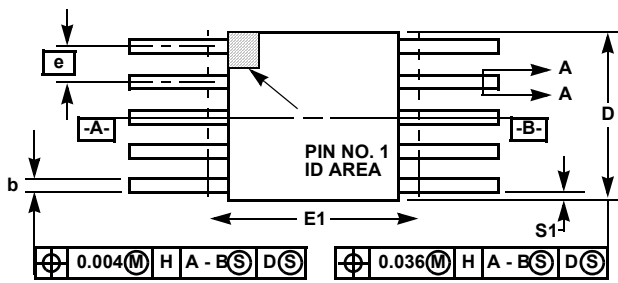
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# ISL70227SEH

## Ceramic Metal Seal Flatpack Packages (Flatpack)



### K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B) 10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

Rev. 0 3/07

#### NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.